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1 Design tradeoffs and experience with Motorola PowerPC migration tools

 Breternitz, M.; Manikonda, A.; Ommerman, M.; Su, W.; Thornton, A.;
 Computer Design: VLSI in Computers and Processors, 1996. ICCD '96.
 Proceedings., 1996 IEEE International Conference on , 7-9 Oct. 1996
 Pages:301 - 308

[\[Abstract\]](#) [\[PDF Full-Text \(748 KB\)\]](#) **IEEE CNF**
2 Software MPEG-2 video decoder on a 200-MHz, low-power multimedia microprocessor

 Nadehara, K.; Lieske, H.; Kuroda, I.;
 Acoustics, Speech, and Signal Processing, 1998. ICASSP '98. Proceedings of the
 1998 IEEE International Conference on , Volume: 5 , 12-15 May 1998
 Pages:3141 - 3144 vol.5

[\[Abstract\]](#) [\[PDF Full-Text \(360 KB\)\]](#) **IEEE CNF**



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1 [Shade: a fast instruction-set simulator for execution profiling](#)

Bob Cmelik, David Keppel

May 1994 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1994 ACM SIGMETRICS conference on Measurement and modeling of computer systems**, Volume 22 Issue 1

Full text available: pdf(1.28 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Tracing tools are used widely to help analyze, design, and tune both hardware and software systems. This paper describes a tool called Shade which combines efficient instruction-set simulation with a flexible, extensible trace generation capability. Efficiency is achieved by dynamically compiling and caching code to simulate and trace the application program. The user may control the extent of tracing in a variety of ways; arbitrarily detailed application state information may be collected ...

2 [Is there an algebraic proof for \$P \neq NC\$? \(extended abstract\)](#)

Ketan Mulmuley

May 1997 **Proceedings of the twenty-ninth annual ACM symposium on Theory of computing**

Full text available: pdf(1.44 MB)

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3 [A solution to the extended GCD problem with applications](#)

Arne Storjohann

July 1997 **Proceedings of the 1997 international symposium on Symbolic and algebraic computation**

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4 [A linear time algorithm for residue computation and a fast algorithm for division with a sparse divisor](#)






Michael Kaminski

October 1987 **Journal of the ACM (JACM)**, Volume 34 Issue 4

Full text available: pdf(1.27 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#), [review](#)


An algorithm is presented to compute the residue of a polynomial over a finite field of degree n modulo a polynomial of degree $O(\log n)$ in $O(n)$ algebraic operations. This algorithm can be implemented on a Turing machine. The implementation is based on Turing machine procedure that divides a polynomial of degree n by a sparse polynomial with k nonzero coeffi ...

- 5 Asymptotically fast computation of Hermite normal forms of integer matrices ☐
Arne Storjohann, George Labahn
October 1996 **Proceedings of the 1996 international symposium on Symbolic and algebraic computation**
Full text available:  [pdf\(775.51 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)
- 6 Fast computation of the Smith normal form of an integer matrix ☐
Mark Giesbrecht
April 1995 **Proceedings of the 1995 international symposium on Symbolic and algebraic computation**
Full text available:  [pdf\(994.43 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)
- 7 Fast algorithms for rational forms of integer matrices ☐
Mark Giesbrecht
August 1994 **Proceedings of the international symposium on Symbolic and algebraic computation**
Full text available:  [pdf\(832.34 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)
- 8 Factor refinement ☐
Eric Bach, James Driscoll, Jeffrey Shallit
January 1990 **Proceedings of the first annual ACM-SIAM symposium on Discrete algorithms**
Full text available:  [pdf\(1.13 MB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)
- 9 Univariate polynomials: nearly optimal algorithms for factorization and rootfinding ☐
Victor Y. Pan
July 2001 **Proceedings of the 2001 international symposium on Symbolic and algebraic computation**
Full text available:  [pdf\(1.32 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)
- To approximate all roots (zeros) of a univariate polynomial, we develop two effective algorithms and combine them in a single recursive process. One algorithm computes a basic well isolated zero-free annulus on the complex plane, whereas another algorithm numerically splits the input polynomial of the n -th degree into two factors balanced in the degrees and with the zero sets separated by the basic annulus. Recursive combination of the two algorithms leads to recursive computation of t ...
- Keywords:** Graeffe's lifting, Padé approximation, computational complexity, geometry of polynomial zeros, numerical polynomial factorization, rootfinding, univariate polynomials

Efficient parallel solution of sparse systems of linear diophantine equations

Mark Giesbrecht

July 1997 **Proceedings of the second international symposium on Parallel symbolic computation**

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11 Fast algorithms for Taylor shifts and certain difference equations

Joachim von zur Gathen, Jürgen Gerhard

July 1997 **Proceedings of the 1997 international symposium on Symbolic and algebraic computation**

Full text available:  pdf(1.07 MB)

Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)



12 An analysis of Lehmer's Euclidean GCD algorithm

Jonathan Sorenson

April 1995 **Proceedings of the 1995 international symposium on Symbolic and algebraic computation**

Full text available:  pdf(510.43 KB)

Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)



13 Note on probabilistic algorithms in integer and polynomial arithmetic

Michael Kaminski

August 1981 **Proceedings of the fourth ACM symposium on Symbolic and algebraic computation**

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For many computational problems it is not known whether verification of a result can be done faster than its computation. For instance, it is unknown whether the verification of the validity of the integer equality $x*y \equiv z$ needs fewer bit operations than a computation of the product $x*y$. It is sometimes much easier, however, to speed up the computation probabilistically if just the verification of the result is involved. In this paper we present linear probabilistic algorithm ...



14 Diophantine linear system solving

Thom Mulders, Arne Storjohann

July 1999 **Proceedings of the 1999 international symposium on Symbolic and algebraic computation**

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15 Lightweight shared objects in a 64-bit operating system

Jeffrey S. Chase, Henry M. Levy, Edward D. Lazowska, Miche Baker-Harvey

October 1992 **ACM SIGPLAN Notices , conference proceedings on Object-oriented programming systems, languages, and applications**, Volume 27 Issue 10

Full text available:  pdf(2.08 MB)

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16 Fast compilation for pipelined reconfigurable fabrics

Mihai Budiu, Seth Copen Goldstein

February 1999 **Proceedings of the 1999 ACM/SIGDA seventh international symposium**



on Field programmable gate arrays

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17 [Near optimal algorithms for computing Smith normal forms of integer matrices](#)

Arne Storjohann

October 1996 **Proceedings of the 1996 international symposium on Symbolic and algebraic computation**


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18 [Performance evaluation and improvement of a dynamically microprogrammable computer with low-level parallelism](#)

Shinji Tomita, Kiyoshi Shibayama, Toshiaki Kitamura, Hiroshi Hagiwara

November 1980 **Proceedings of the 13th annual workshop on Microprogramming**

Full text available:  pdf(1.21 MB)

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A new microprogrammable computer with low-level parallelism was built and has been utilized as a research vehicle for solving different classes of research-oriented applications such as real-time processings on static/dynamic images, pictures and signals, and emulations of both existing and virtual machines including high (intermediate) level language machines. The design goal of a research-oriented computer, QA-1, was to achieve a high degree of processing power and system flexi ...

19 [Technical columns: Routing in distributed networks: overview and open problems](#)

Cyril Gavoille

March 2001 **ACM SIGACT News**, Volume 32 Issue 1

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20 [Factoring modular polynomials \(extended abstract\)](#)

Joachim von zur Gathen, Silke Hartlieb

October 1996 **Proceedings of the 1996 international symposium on Symbolic and algebraic computation**

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"Optimizing a fast stream cipher for VLIW, SIMD, and superscalar processors, Fast Software Encryption, standard.pictel.com/ftp/research/security/widerwake.pdf

[Cameron: High Level Language Compilation for.. - Hammes, Rinker.. \(1999\) \(Correct\) \(3 citations\)](#)

better computational density (the number of **bit operations** a device can perform per unit of area-time) a high level, algorithmic language and optimizing **compiler** for the development of image processing the clock speeds of current FPGAs are slower than **RISC** processor clocks, the potential massive www.cs.colostate.edu/~najjar/papers/pact99.pdf

[Value-Based Clock Gating and Operation Packing: Dynamic.. - Brooks, Martonosi \(2000\) \(Correct\) \(2 citations\)](#)

parallelism, in which multiple 8- or 16-**bit operations** are performed in parallel by a 64-bit ALU, is of their applications in assembler. Little **compiler** support exists to generate them automatically, Architectures]Single Data Stream Architectures-RISC/CISC, VLIW architectures General Terms: Design, www.ee.princeton.edu/~dbrooks/tocs2000.pdf

[Parallel Application Software on High Performance.. - Allan, Bush, Lockey.. \(1996\) \(Correct\) \(2 citations\)](#)

of items 1-4 is shown in Table 1.1 64-**bit operations** are assumed and this is classed as one word of the system. One imagines that the aim of **compiler** writers must be to approach the BLAS performance be based on vector or scalar pipelined (usually **RISC**) processors. The BLAS represent a fundamental www.dl.ac.uk/TCSC/Subjects/Parallel_Algorithms/BLASreport/blas.ps

[Designing the Low-Power M*CORE Architecture - Scott, Lee, Arends, Moyer \(1998\) \(Correct\) \(2 citations\)](#)

provided, as well as instruction support for **bit operations**, byte extraction, data movement, and control derivatives of existing architectures [1,15]**compiler** and compression optimizations [16,17]enhanced length instruction format, and a 32-bit Load/Store **RISC** architecture. The result is high code density www.mot.com/SPS/MCORE/MPU/designwp.pdf

[Sassy: A Language and Optimizing Compiler for Image.. - Hammes, Draper, Böhm \(1999\) \(Correct\) \(1 citation\)](#)

better computational density #the number of **bit operations** a device can perform per unit of area-time# Sassy: A Language and Optimizing **Compiler** for Image Processing on Recon#gurable Computing the clock speeds of current FPGAs are lower than **RISC** processor clocks, the potential massive www.cs.colostate.edu/~draper/publications/hammes_icvs99.pdf

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such as reductions and parallel prefix, global **bit operations** such as logical OR, and barrier compiled to an object module using a traditional **compiler**. The final link stage, however, is performed by processing nodes each based on industrystandard **RISC** microprocessor technology. Each processing node www.media.mit.edu/~mikeb/cmmd-io-paper.ps

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7. <http://wwwbrauer.informatik.tu-muenchen.de/ftp/pub/Alpha/technical-summary.txt> 
ALPHA ARCHITECTURE TECHNICAL SUMMARY Dick Sites, Rich Witek [NOTE: "Alpha" is an internal code nam particular emphasis on speed, multiple **instruction** issue, multiple processors ... of 32- and 64-bit **operations**. Int
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10. <http://www.cs.cmu.edu/~scandal/info/Dec.Alpha> 
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11. <http://burks.bton.ac.uk/burks/pcinfo/hardware/cpu.htm> 
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12. <http://www.cetusm.com/resources/cpuinfo.htm> 
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 the goals of having a no-... user logic, a modern, pipelined **RISC** architecture, and a compiler-friendly **instruction**
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18. <http://www.fh-augsburg.de/informatik/professoren/maertin/rechnerarchitekturen/anhange/literatur/20Microprocessors%20of%20the%20Past%20and%20Present%20%28V%2011.4.3%29.html>
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20. [pa-risc 2.0 instruction set architecture \(HTML\) - HP DSPP](#) 
 Online version of Gerry Kane's PA-**RISC** 2.0 Architecture book. Includes added support for 64-bit computing, perf

operations generate the conditions shown in Table D-15 ...

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Alpha Processors

... although it has a few 32-bit **operations** for backward ... is a 64-bit load/store **RISC** architecture designed ... interact with each other by one **instruction** writing to a ...

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... Whereas a **RISC instruction** on a conventional processor can load ... the load time of an FPGA **instruction** can be ... density" as the number of **bit operations** a device ...

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... in the fact that we are talking about a **RISC** microcontroller whose ... and CLRW writes constant 0 in register W. SWAPF **instruction** exchanges places ... **Bit operations**. ...

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... Given these advantages, compilers for **RISC** machines can ... The MMX **instruction** set extensions offer some hope. They provide 64-bit **operations**, an extra ANDNOT ...

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Code compression under the microscope

... ARC's compilers now emit 16-bit **operations** by default whenever possible ... Those **RISC** architectures (along with PowerPC) have no bit in the **instruction** word to ...

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... in different addressing modes, unlike a **RISC** processor, the ... doesn't fit to the **instruction** at all ... Efficient 64-bit **operations**: The Java bytecode contains 64-bit ...

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